LAB 02

COS10004 – Computer system

CONG THANH NGO

2021

**4 – bit Adder**

Diagram

Description automatically generated

Diagram

Description automatically generated

Diagram, schematic

Description automatically generated

|  |  |  |
| --- | --- | --- |
| **Input A** | **Input B** | **Output** |
| **0101** | 0000 | 0101 |
| **0101** | 0001 | 0110 |
| **0101** | 0010 | 0111 |
| **0101** | 0011 | 1000 |
| **0101** | 0100 | 1001 |
| **0101** | 0101 | 1010 |
| **0101** | 0110 | 1011 |
| **0101** | 0111 | 1100 |
| **0101** | 1000 | 1101 |
| **0101** | 1001 | 1110 |
| **0101** | 1010 | 1111 |
| **0101** | 1011 | 0000 |
| **0101** | 1100 | 0001 |
| **0101** | 1101 | 0010 |
| **0101** | 1110 | 0011 |
| **0101** | 1111 | 0100 |

**RS Flip - Flop**

Diagram

Description automatically generated

Diagram

Description automatically generated

Diagram

Description automatically generatedDiagram

Description automatically generated

|  |  |  |  |
| --- | --- | --- | --- |
| **SET** | **RESET** | **Q** | **Q’** |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 |

Describe in a sentence, the behavior of the circuit when one of the inputs is 1 (but not both) and why this is useful for digital circuit design.

The RS Flip Flop is constructed by linked NOR gates that have been crossed in the diagram above. If we open the Set (1) and close the Reset (0), the Q (1) and Q' will be set (0). In contrast, if we open the Reset (1) and shut the Reset (0), the Not Q or Q' (1) and Q (0) will be set, and the Q will be reset.

What do you notice about the two times you set both inputs to 1. Briefly explain what is happening here and why this is an issue for digital circuit design ?

When we set both inputs Set (1) and Reset (1) to 0, the outputs are both 0 and the RS Flip Flop returns to the undefine state.

This is a problem for digital circuit design since the rule of the flip flop is that the outputs must support and supplement each other. As a result, by being established in this manner, it violates the rule.

**D Flip – Flop**

Diagram, schematic

Description automatically generated

Diagram

Description automatically generated

Diagram, schematic

Description automatically generated

Diagram, schematic

Description automatically generated

|  |  |  |  |
| --- | --- | --- | --- |
| Clock | Pin | Q | Q’ |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |

Briefly explain the behavior of a D Flip Flop and how it is useful for digital circuit design

The D Flip-Flop has a single data input and uses the clock to regulate the signal. When the clock starts, Q is set to be inverted as D, and Not Q or Q' is set to be the same as D.

What is the role of the clock? How does it impact the changing of state of Q and Q’?

The clock is used to send a signal to the control signal. When the clock signal is LOW, the input has no effect on the output. However, for the inputs to become active, the clock signal must be HIGH.

Why is it generally preferred over the R-S Flip Flop?

The D flip-flop is chosen over the R-S flip-flop because it helps to synchronize data in situations when everything must be timed, and the D flip-flop has that benefit. D flip-flop for serial-to-parallel conversion, non-standard counters, frequency division, and without the additional pins required in SR flip-flops.

**JK Flip – Flop**

Diagram, schematic

Description automatically generated

Diagram, schematic

Description automatically generated

Diagram, schematic

Description automatically generated

|  |  |  |  |
| --- | --- | --- | --- |
| **J** | **K** | **Q(Clocked)** | **Q’(Clock)** |
| 0 | 0 | No change |  |
| 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 1 | Toggle |  |

How can a J-K Flip Flop be made to behave like a D Flip Flop?

A JK flip-flop may be turned into a D flip-flop by driving its J and K input pins with the D input. A NOT gate is required as an extra hardware component.

|  |  |  |
| --- | --- | --- |
| **D** | **Qn** | **Qn+1** |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

How can a J-K Flip Flop be made to behave like a toggle (T Flip Flop)?

When both J and K inputs are 1, the J-K Flip Flop behaves as a toggle.